# HCPL-8100/0810
High Current Line Driver

## Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

### Description

The HCPL-8100 and HCPL-0810 are low-cost high current line drivers. With a 5 V single supply, they deliver up to 1 $A_{PP}$ current. This is ideal for high current applications such as a Powerline modem.

The HCPL-8100 and HCPL-0810 are internally protected against over-temperature conditions through thermal shutdown. Under-voltage or over-load condition is sensed by internal detection circuit and indicated by Status pin output. In addition, with the transmit enable (Tx-en) input, the line driver output stage can be disabled to reduce power dissipation when not operating.

The HCPL-8100 and HCPL-0810 are specified for operation over extended temperature range from -40°C to +85°C. The HCPL-8100 is available in DIP-8 package, and the HCPL-0810 is available in SO-8 package.

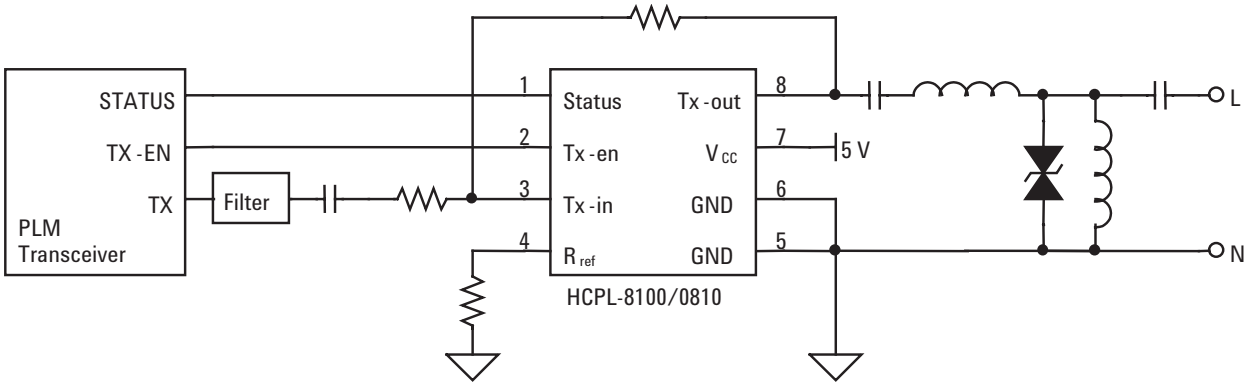
### Features

- 1 $A_{PP}$ driving current
- 3.5 MHz gain bandwidth product
- - 60 dB maximum harmonic distortion
- Load detection function
- Under-voltage detection
- Over-temperature shutdown
- 5 V single supply
- Temperature range: -40°C to +85°C
- Suitable for FCC Part 15 and EN50065-1 compliant design

### Applications

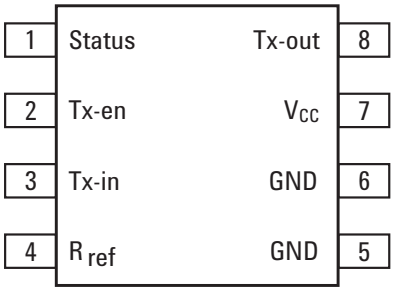
- Automatic meter reading (AMR)
- Powerline modem
- General purpose line driver
- Signal conditioning
- Digital-to-analog converter buffers

### Connection Diagram




*CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and /or degradation which may be induced by ESD.*

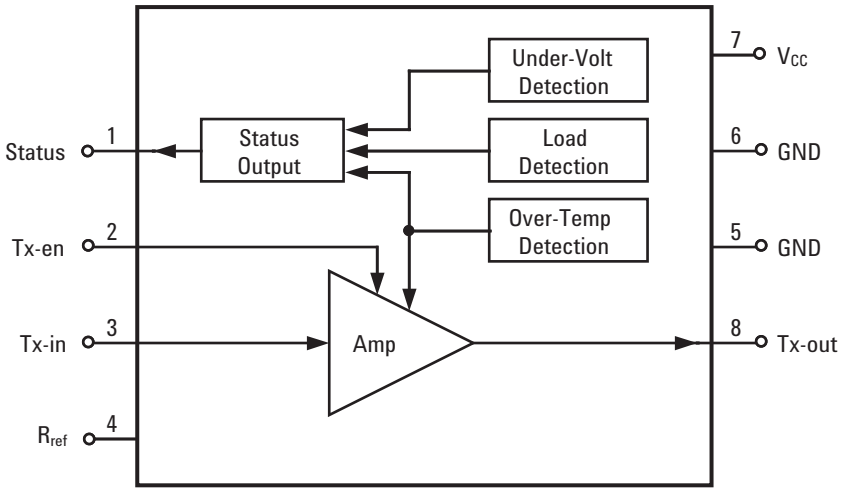
## Package Pin Out




## Pin Descriptions

| Pin No. | Symbol | Function | Description |
|---|---|---|---|
| 1 | Status | Line condition detection | A logic high indicates line conditions such as- under-voltage when $V_{CC} < 4$ V- load detection when $I_{Tx\text{-}out} < -0.25$ A- over-temperature (thermal shutdown) |
| 2 | Tx-en | Transmit enable | A logic high enables the Tx-out;A logic low disables the Tx-out and changes it to high impedance state |
| 3 | Tx-in | Transmit input | Transmit signal input |
| 4 | $R_{ref}$ | Resistor reference | Sets line driver biasing current, typically 24 kΩ |
| 5, 6 | GND | Power supply ground | Power supply and signal ground |
| 7 | $V_{CC}$ | 5 V power supply | 5 V power supply |
| 8 | Tx-out | Transmit output | Transmit signal output, to be enabled by Tx-en |

## Block Diagram




## Ordering Information

| | Option | | | | |
|---|---|---|---|---|---|
| Part number | RoHS Compliant | Packaging | Surface Mount | Tape & Reel | Quantity |
| HCPL-0810 | -000E | SO-8 | X | | 100 per tube |
| | -500E | SO-8 | X | X | 1500 per reel |
| HCPL-8100 | -000E | 300mil DIP-8 | | | 50 per tube |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-0810-500E to order product of SO-8 package in Tape and Reel packaging and RoHS compliant.

Example 2:

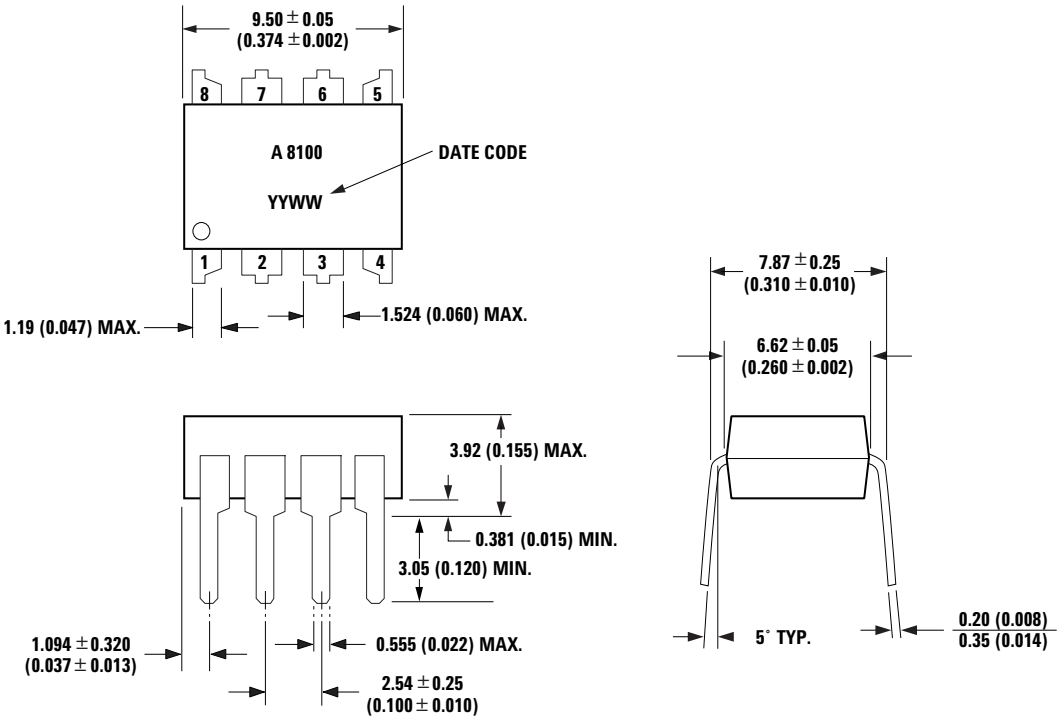
HCPL-8100-000E to order product of 300mil DIP-8 package in Tube packaging and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

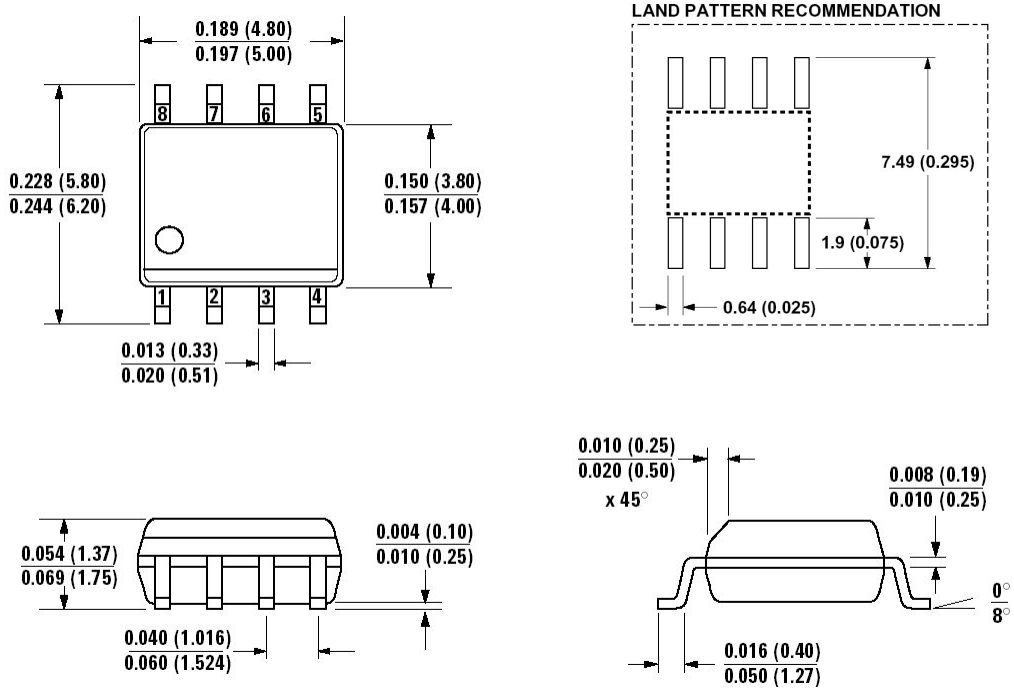
## Package Outline Drawings

HCPL-8100 Standard 8-pin DIP package



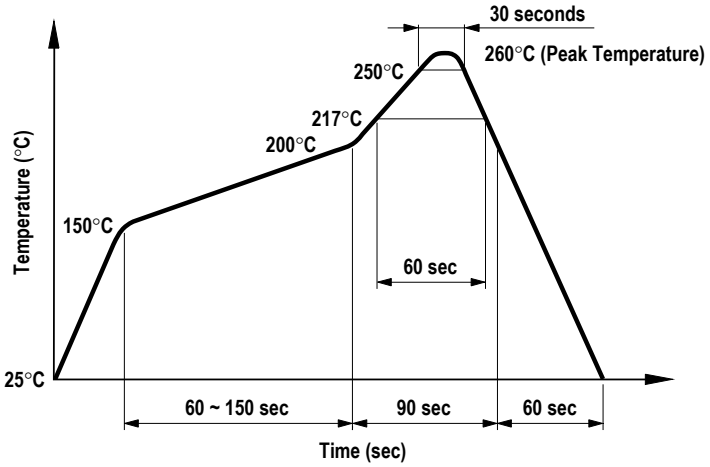

DIMENSIONS IN MILLIMETERS AND (INCHES)

HCPL-0810 Small Outline SO-8 Package




DIMENSIONS IN MILLIMETERS AND (INCHES)

## Recommended Pb-free IR Profile




Note: Non-halide flux should be used

## Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Storage Temperature | $T_S$ | -55 | 125 | °C |
| Ambient Operating Temperature | $T_A$ | -40 | 85 | °C |
| Junction Temperature | $T_J$ | | 150 | °C |
| Supply Voltage | $V_{CC}$ | -0.5 | 5.5 | Volts |
| Output Voltage | $V_O$ | -0.5 | $V_{CC}$ | Volts |
| Tx-in Voltage | $V_{Tx\text{-}in}$ | -0.5 | $V_{CC}$ | Volts |
| Tx-en Voltage | $V_{Tx\text{-}en}$ | -0.5 | $V_{CC}$ | Volts |
| Solder Reflow Temperature Profile | (See Solder Reflow Temperature Profile Section) | | | |

## Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Ambient Operating Temperature | $T_A$ | -40 | 25 | 85 | °C |
| Supply Voltage | $V_{CC}$ | 4.75 | 5 | 5.25 | V |

## Electrical Specifications

Unless otherwise noted, for sinusoidal waveform input and reference resistor $R_{ref}$ = 24 kΩ, all typical values are at $T_A$ = 25°C and $V_{CC}$ = 5 V; all Minimum/Maximum specifications are at Recommended Operating Conditions.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Condition | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ Supply Current | $I_{CC}$ | | 1.2 | 2 | mA | $V_{Tx-en}$ = 0 V, $V_{Tx-in}$ = 0 $V_{PP}$, Tx-out no load | 1 | |
| | | | 20 | 45 | mA | $V_{Tx-en}$ = 5 V, $V_{Tx-in}$ = 0 $V_{PP}$, Tx-out no load | 2, 3 | |
| $V_{CC}$ Under Voltage Detection | $V_{UVD}$ | 3.8 | 4.0 | 4.3 | V | | | 1 |
| Junction Over-Temperature Threshold | | | 150 | | °C | | | 2 |
| Load Detection Threshold | | | 0.5 | | $A_{PP}$ | $V_{Tx-en}$ = 5 V, $V_{Tx-in}$ = 1.25 $V_{PP}$, f = 132 kHz, Gain = – 2, $R_L$ = 2.5 Ω | 12, 13 | 3 |
| Status Logic High Output | $V_{OH}$ | $V_{CC}$–1 | | $V_{CC}$ | V | $V_{CC}$ = 3.5 V, $I_{OH}$ = – 4 mA | | |
| Status Logic Low Output | $V_{OL}$ | 0 | | 0.8 | V | $V_{CC}$ = 5 V, $I_{OL}$ = 4 mA | | |
| Power Supply Rejection Ratio | PSRR | | 72 | | dB | 50 Hz ripple, $V_{ripple}$ = 200 $mV_{PP}$, $V_{Tx-en}$ = 5 V, $V_{Tx-in}$ = 0 $V_{PP}$, Tx-out no load | | |
| DC Bias Voltage | $V_{Bias}$ | | 2.27 | | V | $V_{Tx-en}$ = 5 V, Tx-out no load | | |
| Output Impedance | $Z_O$ | | 12 | | kΩ | $V_{Tx-en}$ = 0 V, $V_{Tx-in}$ = 0 $V_{PP}$, open loop, f = 132 kHz | | |
| | | | 0.5 | | Ω | $V_{Tx-en}$ = 5 V, $V_{Tx-in}$ = 0 $V_{PP}$, f = 132 kHz | | |
| Gain Bandwidth Product | GBW | | 3.5 | | MHz | $V_{Tx-en}$ = 5 V, $V_{Tx-in}$ = 1 $V_{PP}$, $R_L$ = 50 Ω | 4, 14 | |
| Transmit Enable Threshold Voltage | $V_{th, Tx}$ | 0.8 | | 2.4 | V | $V_{Tx-in}$ = 1 $V_{PP}$, f = 132 kHz, Tx-out no load | | |
| Tx Enable Time | $t_{Tx-en}$ | | 0.9 | | µs | $V_{Tx-en}$ = 5 V, $V_{Tx-in}$ = 1.75 $V_{PP}$, f = 132 kHz, Tx-out no load | 11, 15 | |
| Tx Disable Time | | | 0.2 | | µs | $V_{Tx-en}$ = 0 V, $V_{Tx-in}$ = 1.75 $V_{PP}$, f = 132 kHz, Tx-out no load | 15 | |
| 2nd Harmonic Distortion | HD2 | | –65 | –60 | dB | $V_{Tx-en}$ = 5 V, $V_{Tx-out}$ = 3.5 $V_{PP}$, f = 132 kHz,Gain = –2, $R_{ref}$ = 24 k Ω, $R_L$= 50 Ω | 5-10, 16 | |
| 3rd Harmonic Distortion | HD3 | | –75 | –65 | dB | | | |
| Output Current | $I_O$ | | 1 | | $A_{PP}$ | $V_{Tx-en}$ = 5 V, f=132 kHz | | 4 |
| Thermal Resistance (HCPL-8100) | $\theta_{JA}$ | | 100 | | °C/W | 1 oz. trace, 2-layer PCB, still air, $T_A$ = 25°C | | |
| | | | 60 | | °C/W | 1 oz. trace, 4-layer PCB, still air, $T_A$ = 25°C | | |
| Thermal Resistance (HCPL-0810) | $\theta_{JA}$ | | 138 | | °C/W | 1 oz. trace, 2-layer PCB, still air, $T_A$ = 25°C | | |
| | | | 70 | | °C/W | 1 oz. trace, 4-layer PCB, still air, $T_A$ = 25°C | | |

Notes:
1. Threshold of falling $V_{CC}$ with hysteresis of 0.2 V (typ.).
2. Threshold of rising junction temperature with hysteresis of 20°C (typ.).
3. See Application Information section for more information on the load detection feature.
4. See Figure 3 for the plot of supply current versus Tx output current.

## Performance Plots

Unless otherwise noted, all typical plots are at $T_A$ = 25°C, $V_{CC}$ = 5 V, sinusoidal waveform input and $R_{ref}$ = 24 kΩ.

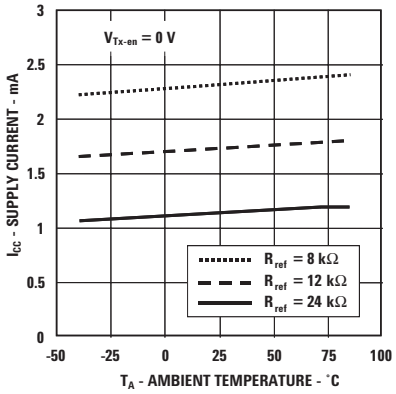



Figure 1. Supply current vs. temperature for Tx disabled.

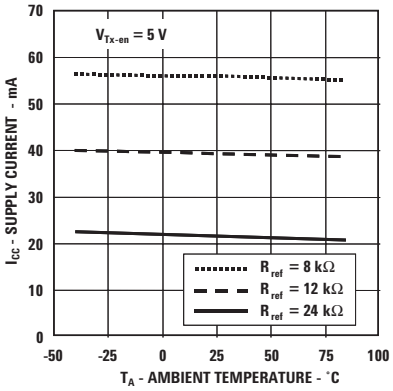



Figure 2. Supply current vs. temperature for Tx enabled.

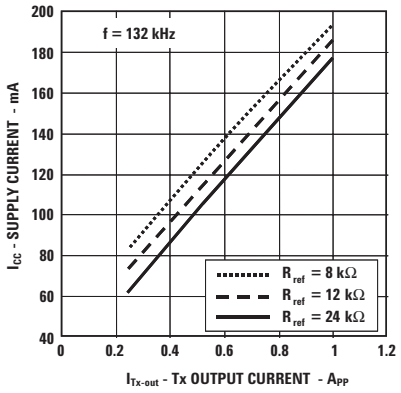



Figure 3. Supply current vs. Tx output current.

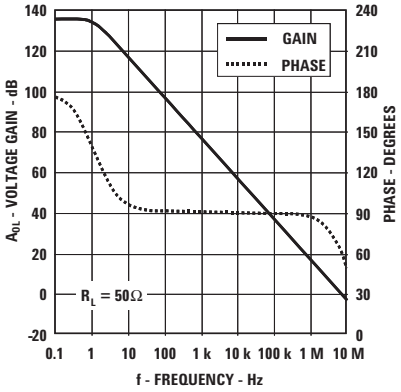



Figure 4. Gain and phase vs. frequency.

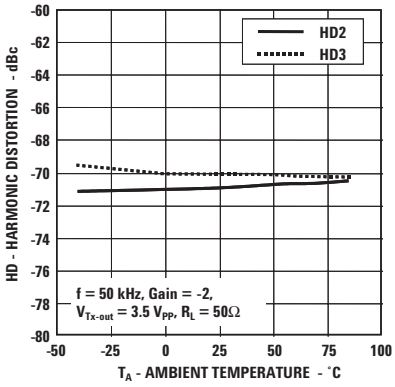



Figure 5. Tx-out harmonic distortion vs. temperature for f = 50 kHz.

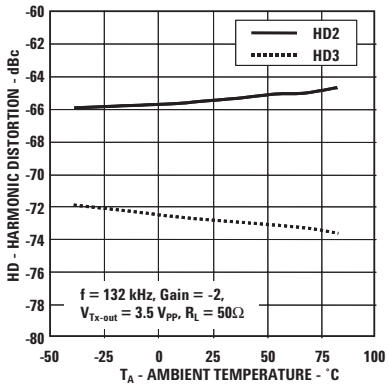



Figure 6. Tx-out harmonic distortion vs. temperature for f = 132 kHz.

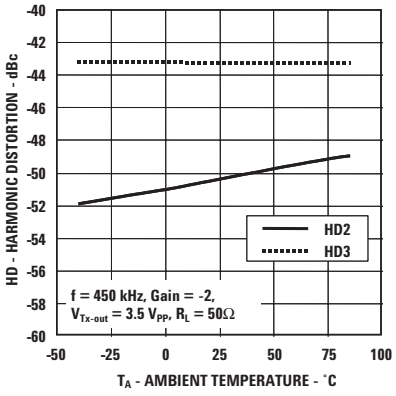



Figure 7. Tx-out harmonic distortion vs. temperature for f = 450 kHz.

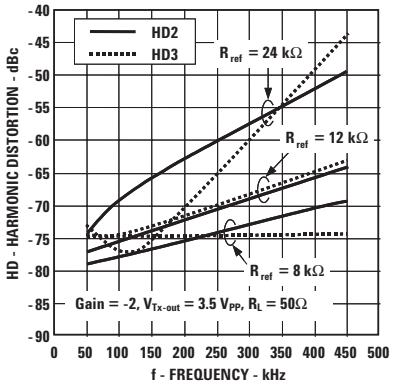



Figure 8. Tx-out harmonic distortion vs. frequency for different values of $R_{ref}$ at Gain = -2.

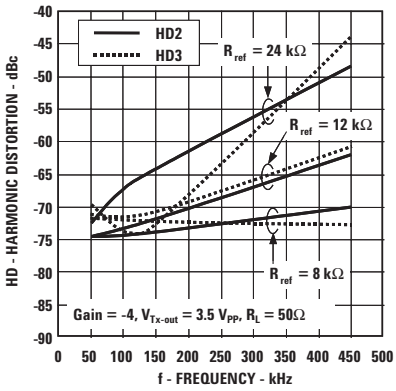



Figure 9. Tx-out harmonic distortion vs. frequency for different values of $R_{ref}$ at Gain = -4.

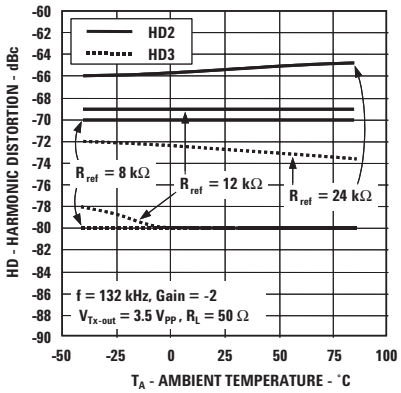



**Figure 10. Tx-out harmonic distortion vs. temperature for different values of $R_{ref}$.**

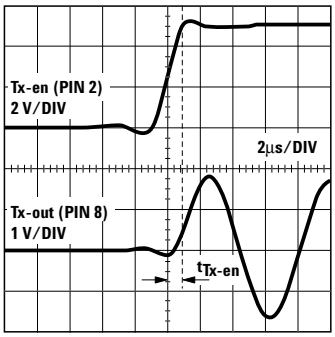



**Figure 11. Tx enable time.**

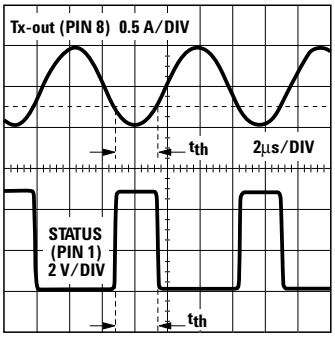



**Figure 12. Tx-out load detection.**

## Test Circuit Diagrams

Unless otherwise noted, all test circuits are at $T_A$ = 25°C, $V_{CC}$ = 5 V, sinusoidal waveform input, and signal frequency f = 132 kHz.

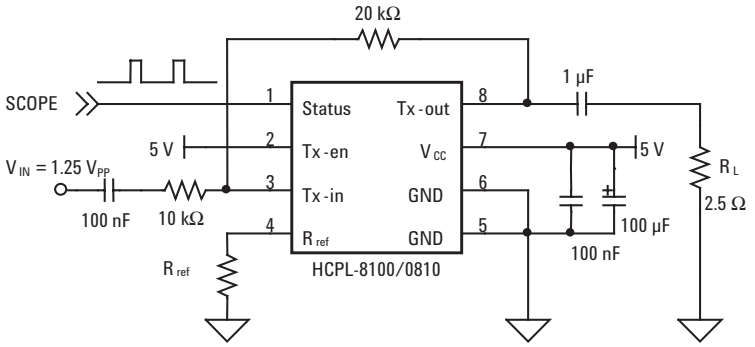



**Figure 13. Load detection test circuit.**

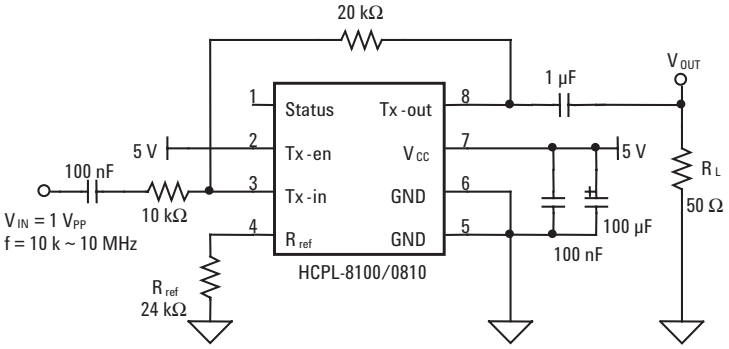



**Figure 14. Gain bandwidth product test circuit.**

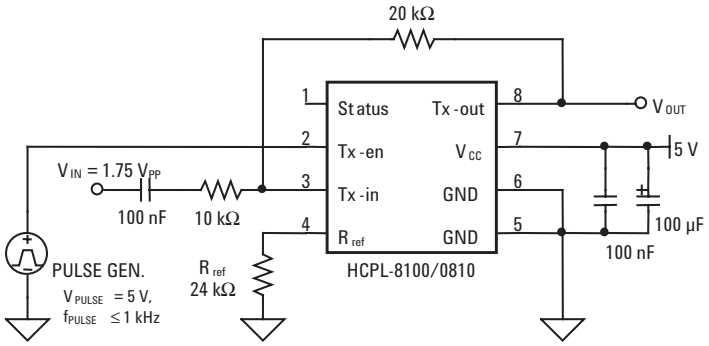



**Figure 15. Tx enable/disable time test circuit.**

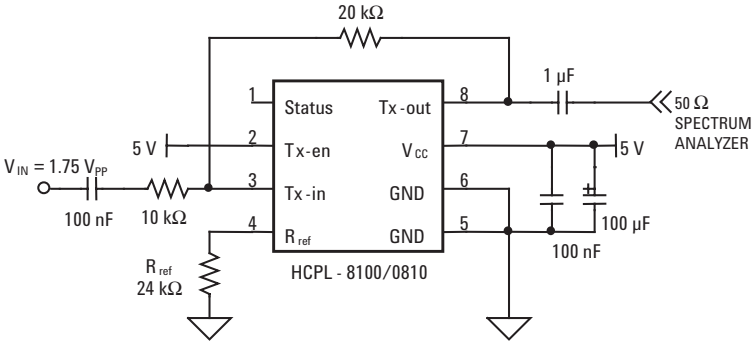



**Figure 16. Tx-out harmonic distortion test circuit.**

## Application Information

The HCPL-8100 and HCPL-0810 are designed to work with various transceivers and can be used with a variety of modulation methods including ASK, FSK and BPSK. Figure 17 shows a typical application in a powerline modem using Frequency Shift Keying (FSK) modulation scheme.

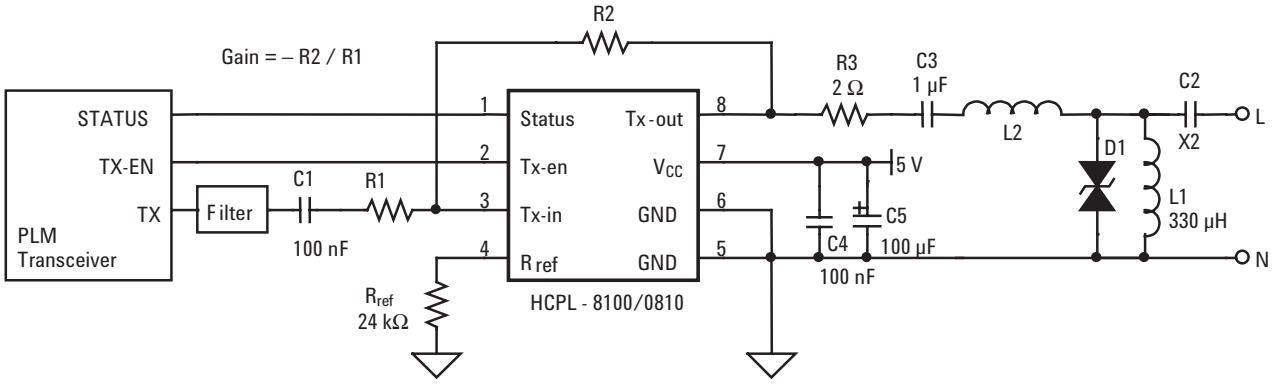



**Figure 17. Schematic of HCPL-8100 or HCPL-0810 application for FSK modulation scheme.**

## Line Driver

The line driver is capable of driving powerline load impedances with output signals up to 4 $V_{PP}$. The internal biasing of the line driver is controlled externally via a resistor $R_{ref}$ connected from pin 4 to ground. The optimum biasing point value for modulation frequencies up to 150 kHz is 24 kΩ. For higher frequency operation with certain modulation schemes, it may be necessary to reduce the resistor value to enable compliance with international regulations.

The output of the line driver is coupled onto the powerline using a simple LC coupling circuit as shown in Figure 18. Refer to Table 1 for some typical component values. Capacitor C2 and inductor L1 attenuate the 50/60 Hz powerline transmission frequency. A suitable value for L1 can range in value from 200 µH to 1 mH. To reduce the series coupling impedance at the modulation frequency, L2 is included to compensate the reactive impedance of C2. This inductor should be a low resistive type capable of meeting the peak current requirements. To meet many regulatory requirements, capacitor C2 needs to be an X2 type. Since these types of capacitors typically have a very wide tolerance range of 20%, it is recommended to use as low Q factor as possible for the L2/C2 combination. Using a high Q coupling circuit will result in a wide tolerance on the overall coupling impedance, causing potential communication difficulties with low powerline impedances. Occasionally with other circuit configurations, a high Q coupling arrangement is recommended, e.g., C2 less than 100 nF. In this case it is normally used as a compromise to filter out of band harmonics originating from the line driver. This is not required with the HCPL-8100 or HCPL-0810.

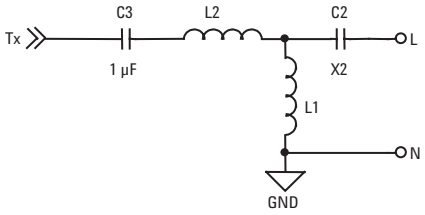



**Figure 18. LC coupling network.**

**Table 1. Typical component values for LC coupling network.**

| Carrier Frequency (kHz) | LC Coupling | |
|---|---|---|
| | L2 (µH) | C2 (nF) |
| 110 | 15 | 150 |
| 120 | 10 | 220 |
| 132 | 6.8 | 220 |
| 150 | 6.8 | 220 |

Although the series coupling impedance is minimized to reduce insertion loss, it has to be sufficiently large to limit the peak current to the desired level in the worst expected powerline load condition. The peak output current is effectively limited by the total series coupling resistance, which is made up of the series resistance of L2, the series resistance of the fuse and any other resistive element connected in the coupling network.

To reduce power dissipation when not operating in transmit mode the line driver stage is shut down to a low power high impedance state by pulling the Tx-en input (pin 2) to logic low state.

## External Transient Voltage Protection

To protect the HCPL-8100 and HCPL-0810 from high voltage transients caused by power surges and disconnecting/connecting the modem, it is necessary to add an external 6.8 V bi-directional transient voltage protector (as component D1 shown in Figure 17).

Additional protection from powerline voltage surges can be achieved by adding an appropriate Metal Oxide Varistor (MOV) across the powerline terminals after the fuse.

## Internal Protection and Sensing

The HCPL-8100 and HCPL-0810 include several sensing and protection functions to ensure robust operation under wide ranging environmental conditions.

The first feature is the $V_{CC}$ Under Voltage Detection (UVD). In the event of $V_{CC}$ dropping to a voltage less than 4 V, the output status pin is switched to a logic high state.

The next feature is the over-temperature shutdown. This particular feature protects the line driver stage from over-temperature stress. Should the IC junction temperature reach a level above 150°C, the line driver circuit will be shut down and the output of Status (pin 1) is pulled to the logic high state simultaneously.

The final feature is load detection function. The powerline impedance is quite unpredictable and varies not just at different connection points but is also time variant. The HCPL-8100 and HCPL-0810 include a current sense feature, which may be utilized to feedback information on the instantaneous powerline load condition. Should the peak current reach a level greater than 0.5 $A_{PP}$, the output of status pin is pulled to a logic high state for the entire period the peak current exceeds -0.25 A as shown in Figure 12. Using the period of the pulse together with the known coupling impedance, the actual powerline load can be calculated. Table 2 shows the logic output of the Status pin.

**Table 2. Status pin logic**

| | Normal | $V_{CC}$ < 4 V | Over-Temperature | $I_{Tx\text{-}out}$ < – 0.25 A |
|---|---|---|---|---|
| Status output | Low | High | High | High (pulsed) |



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